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Integrated Reconfigurable High-Voltage Transmitting Circuit for CMUTs

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Abstract In this paper a high-voltage transmitting circuit aimed for capacitive micromachined ultrasonic transducers (CMUTs) used in scanners for medical applications is designed and implemented in a 0.35 µm high-voltage CMOS process. The transmitting circuit is reconfigurable externally making it able to drive a wide variety of CMUTs. The transmitting circuit can generate several pulse shapes with voltages up to 100 V, maximum pulse range of 50 V, frequencies up to 5 MHz and different driving slew rates. Measurements are performed on the circuit in order to assess its functionality and power consumption performance. The design occupies an on-chip area of 0.938 mm^2 and the power consumption of a 128-element transmitting circuit array that would be used in an portable ultrasound scanner is found to be a maximum of 181 mW.

Keywords Integrated · Transmitting circuit · High-voltage · Pulser · Level shifter · Output stage · Ultrasound · Scanners · CMUT ·

1 Introduction

Ultrasound imaging systems are widely used in medical applications since it is a cost efficient, ionizing radiation free and noninvasive diagnostic technique that allows real time imaging. The complexity of ultrasound systems has been increasing throughout the years improving further and further the image quality. However a tendency of high integration has enabled portable ultrasound systems with comparable performance to the traditional static ultrasound systems. The main restriction of portable scanners is the limited power budget due to the limited power storage in the battery and/or the heating dissipation capabilities of the device, which sets the maximum current allowed to be spent into the electronics. Furthermore the reduced size of the portable scanners also sets a restriction regarding the area of the electronics. Consequently reducing the power consumption and area of the electronics is the main target when designing integrated circuits for portable ultrasound scanners. In Fig. 1 the typical block structure of an ultrasound system can be seen. The transmitting circuit (Tx) drives the transducer in order to generate the ultrasound, which will be reflected off of the scanned internal tissue and travel back to the transducer inducing a current that is amplified and digitized by the receiving circuit (Rx). The amplified and digitized signal is sent to a signal processing unit to obtain the real time imaging.

Piezoelectric transducers have been typically used in ultrasound systems, but in the last two decades extensive research has proved that capacitive micromachined ultrasonic transducers (CMUTs) are a very suitable al-

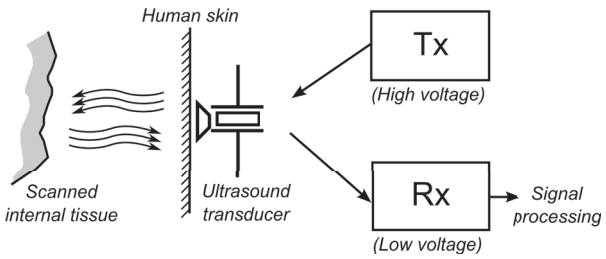

Fig. 1 Typical block structure of an ultrasound system.

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ternative. The performance and the fabrication process are the main advantages of the CMUTs compared to the conventional piezoelectric transducers. CMUTs have a wider bandwidth, which translates into better temporal and axial resolution, and also better thermic and transduction efficiency [1]. Moreover, they also benefit from the standard silicon integrated circuit fabrication technology advantages such as low cost and high flexibility, which allows easier fabrication of large complex transducer arrays. The last advantage of CMUTs is its high integration compatibility with electronic circuits, since CMUTs can be directly bonded with the integrated circuit die or even built on the top of a finished electronic wafer [2].

CMUTs are composed of a thin movable plate suspended on a small vacuum gap on the top of a substrate. The movable plate forms one of the terminals of the transducer and the substrate acts as the second terminal. By applying a voltage difference between those terminals an attractive electrostatic force is generated deflecting the movable plate towards the substrate. Once the plate starts deflecting, a mechanical force is created due to its stiffness which acts against the electrostatic force until a force equilibrium is reached. In order to operate, CMUTs require a stable deflected position hence high bias voltage between its plates in the order of 100 V is needed. However, in transmitting mode, a high-voltage pulse on the top of this bias voltage is applied in order to make the movable plate vibrate generating the ultrasound [3]. These pulses need to be symmetrical with respect to the bias voltage in order to obtain high quality transmitting ultrasonic waves, and the frequency of these pulses need to match the resonant frequency of the CMUT. This high quality transmitting waves will translate into better picture quality, which is the main target of ultrasound scanners. The transmitting circuitry is required to operate in high-voltage, generating the bias voltage and the pulses. The bias voltage and the pulse characteristics, such as amplitude, slew rate and frequency, depend on the specific CMUT to drive, therefore each transmitting circuit has to be designed and adjusted to match the requirements of the transducer. The electrical equivalent of a CMUT load driven at its resonant frequency corresponds is a parallel combination of a capacitance in the order of tens of pico farads and a resistance in the order of tens of kilo ohms. The transmitting circuit needs to handle a maximum peak current to charge and discharge the capacitance of the transducer and an continuous current through the resistance, which corresponds to the energy transmitted to the ultrasonic waves.

An ultrasound scanner contains arrays of up to thousands of CMUTs that each needs a transmitting circuit. Consequently, the power consumption and area of a single transmitting circuit is key in order to make them scalable into a portable hand held scanner. Integrating the transmitting circuit in an ASIC reduces the area and the power consumption of the Tx since it is specifically designed for its application. However, the transmitting circuit requires voltages around hundred volts which can not be handled by standard CMOS processes. The Tx needs to be designed in a high-voltage process which is significantly different from standard ones. These processes have more strict design rules since they require guard-rings and more spacing to avoid high-voltage breakdowns and also use high-voltage devices which are more complex than standard MOS transistors.

This paper deals with the design and implementation of a full integrated reconfigurable transmitting circuit. It is decided to design the transmitting circuit to be reconfigurable in order to drive CMUTs with different characteristics. The bias voltage, pulse amplitude, frequency and shape are going to be adjustable externally. However, this driving flexibility has an area and power consumption cost. Nonetheless, the primary focus of this paper is to design a Tx that can generate a wide variety of driving pulses, so the area and power consumption cost is assumed and acknowledged as not being the main strength of the design. In the future, for the implementation of the Tx in the portable scanner, the area and power consumption can be reduced by designing the circuit for a specific CMUT.

This paper is an extended version of work published in the 32nd Norchip Conference 2014, [4]. It is structured as follows: In Section 2 the specifications of the Tx circuit are defined and the topologies and blocks used to implement it are shown in Section 3. The layout of the integrated circuit and the measurement results can be seen in Section 4 and the conclusions and future work can be found in Section 5 and 6 respectively.

2 Transmitting circuit specifications

The first consideration in order to design a transmitting circuit for CMUTs is the number of voltage levels that the circuit needs to provide. A common and simple way of driving CMUTs is by using two-level output stage [5],[6],[7]. However, in order to achieve high quality transmitting ultrasonic waves and improve picture quality, the pulses sent to the transducer need to be symmetrical with respect to the bias voltage. Therefore, a three-level output stage is needed. In this design, a three-level output stage is used. The high and low voltage levels are used for pulsing and the middle level is only used for biasing the CMUT.

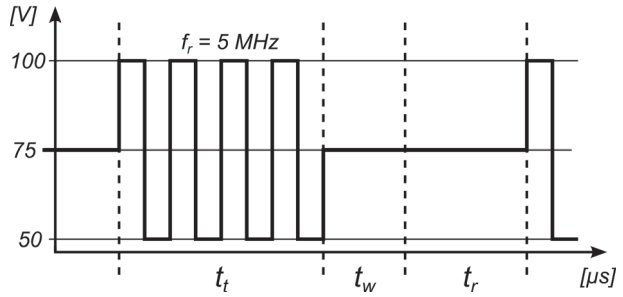

Fig. 2 Full operating cycle of the voltage between terminals of the CMUT.

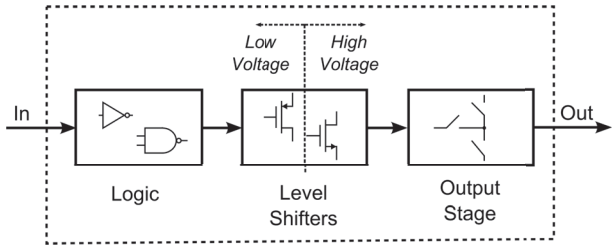

Fig. 3 Block structure of the transmitting circuit.

As it was stated before, the specifications for the transmitting circuit are dictated by the CMUT characteristics. In order to set the specifications for a reconfigurable transmitting circuit the transducer with the most strict driving requirements needs to be defined. The Tx is designed for this transducer while ensuring that it is easily reconfigurable and can function within a range of more relaxed requirements. A CMUT is characterized by its own resonant frequency, bias voltage and pulse amplitude, which correspond to the frequency of the pulses and voltage levels that the Tx circuit needs to generate. The transducer with higher driving requirements that this Tx circuit was targeted to drive has a resonant frequency of $f_r = 5\,\text{MHz}$, bias voltage of 75 V and peak-to-peak pulse amplitude of 50 V, which translates into voltage level generation of 50 V, 75 V and 100 V.

The operating cycle of a transducer consists of a transmitting time, a waiting time and a receiving time. During transmitting time the Tx circuit is required to send to the CMUT pulses on top of the bias voltage. In the waiting and receiving time the Tx circuit only biases the CMUT. Using the previous specifications defined by the most restrictive transducer, the voltage between the terminals of the CMUT for a full operating cycle can be seen in Fig. 2. When transmitting (t_t), the voltage toggles between 50 V and 100 V with a frequency of 5 MHz and during waiting (t_w) and receiving time (t_r) the CMUT is biased at 75 V. This is the most demanding output signal that the transmitting circuit needs to generate. Due to these high-voltage requirements the process used for the implementation of this transmitting circuit is a 0.35 µm high-voltage CMOS process.

3 Design and implementation of the Tx

The block structure of the transmitting circuit designed is shown in Fig. 3. The inputs of the system are low-voltage signals defining the frequency operation, the waiting time (t_w), the transmitting (t_t) and receiving time (t_r), which are transformed by the logic block into the internal signals that the Tx circuit requires. Using the level shifter block, the low-voltage signals are converted into the high-voltage signals that the output stage needs in order to generate the high-voltage output signal for the CMUT described in section 2.

For the design of each block, high-voltage devices with different capabilities are used. In Fig. 4 the specifications and symbols for each device are shown, stating the type of transistor and the maximum voltage levels between terminals. An NMOSI transistor is an isolated NMOS which is located in its own P-well, therefore its bulk terminal can be connected to a different potential than the p-substrate. Note that all the MOS transistors in Fig. 4 and in all the following schematics are assumed to have the body terminal connected to the source.

The transmitting circuit is designed for high-voltage operation therefore some considerations other than the current capability and capacitances of the MOS devices need to be done. Firstly, one of the main considerations in high-voltage design is the lifetime of the devices. Minimum size high-voltage devices are very sensitive to lifetime reduction when operated at maximum voltage conditions and in order to improve this parameter the area of the device has to be increased. This can be done by either over-designing the device by increasing the width to length ratio or by using a device with higher voltage breakdown capabilities than needed. Secondly, since area is an issue, a common practice to shrink the design is to use shared deep N-well for several transistors. However there are some limitations to deep N-well sharing rules in the process used. The high-voltage NMOSI devices can only share deep

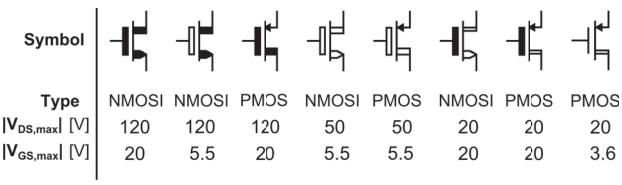

Fig. 4 High-voltage MOS transistors specifications and symbols.

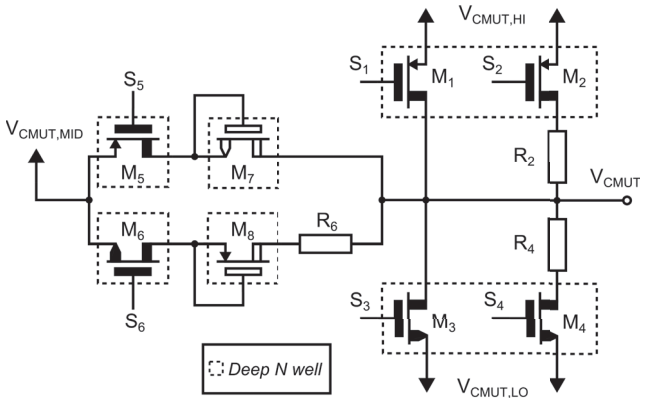

Fig. 5 Schematic of the output stage.

N-well with other MOS devices having the same drain voltage. This is possible since the process provides several deep and shallow wells. Similarly, the high-voltage PMOS devices can only be contained in the same deep N-well with other MOS devices if they have the same source voltage. These deep N-wells are clearly indicated in the schematics of all the designs.

3.1 Output stage

The output stage drives one of the terminals of the CMUT while the second terminal is voltage biased. Since CMUTs are affected by the differential voltage between their plates the main discussion is whether the biased terminal of the transducer should be high-voltage biased or grounded. High-voltage biasing one of the terminals of the CMUT has the advantage of lowering the voltage levels of the CMUT terminal connected to the output stage, hence the circuit requirements are lower and the area and power consumption are reduced. However, ultrasound scanners are used directly onto patients therefore having high voltages towards them can be an issue. Despite the higher voltages necessity in the output stage, in this design the terminal of the CMUT towards the patient was grounded and the output stage operates in the other terminal. This is a system level decision taken for safety reasons and in this work its cost in terms of area and power consumption are investigated.

The schematic of the output stage used can be seen in Fig. 5. Note that upper case notation is used for all the signals of the output stage since they are high-voltage. The output stage consists of six branches that connect an output node (V_{CMUT}) to its different voltage levels. M_1/M_2, M_3/M_4 and M_5/M_6 function as switches connecting the CMUT to $V_{CMUT,HI} = 100\,\mathrm{V}$, $V_{CMUT,LO} = 50\,\mathrm{V}$ and $V_{CMUT,MID} = 75\,\mathrm{V}$ respectively. The only difference between pulling the output node with M_1/M_3 or with M_2/M_4 is the driving speed. The resistors R_2 ($2.1\,\mathrm{k}\Omega$) and R_4 ($2.1\,\mathrm{k}\Omega$) are connected in series with M_2 and M_4 obtaining a slower response of the output node. This is a versatility feature that allows two different driving speeds both for the rising and falling edges of the pulses. The resistor R_6 ($80\,\mathrm{k}\Omega$) connected in series with M_6 is added in order to have a high impedance branch to $V_{CMUT,MID}$ so that the transducer can be voltage biased in receiving mode without affecting the receiving path to the low-voltage Rx circuit.

Three different voltage levels are connected to the same output node therefore two switches (M_5/M_6) connected to $V_{CMUT,MID}$ are required to pull down from $V_{CMUT,HI}$ or pull up from $V_{CMUT,LO}$. In order to avoid short circuiting $V_{CMUT,HI}$ and $V_{CMUT,MID}$ through the body diode of M_5 when the output is $V_{CMUT,HI}$, the transistor M_7 acting as a blocking diode is needed. Similarly, M_8 prevents short circuiting $V_{CMUT,LO}$ and $V_{CMUT,MID}$ through the body diode of M_6 when the output voltage is $V_{CMUT,LO}$.

The high-voltage signals S_1, S_2, S_3, S_4, S_5 and S_6 in Fig. 5 control which of the output stage MOS transistors is on at every part of the transmitting-receiving cycle (Fig. 2). It is important to notice that only one of the MOS transistors should be on at a time, otherwise two voltage supplies are going to be shorted and a large current is going to be wasted while potentially destroying the MOS transistors. During transmission (t_t) M_1/M_2 and M_3/M_4 are inversely toggled on and off, in the waiting time (t_w) only M_5 is turned on and in receiving time (t_r) only M_6 is turned on.

The load equivalent of the CMUT consists of a capacitive and a resistive component. The capacitive component needs to be charged and discharged during transmission, and the resistive component power dissipation corresponds to the energy transferred to the ultrasonic waves. The most restrictive current, regarding the output stage design, is the peak current to charge and discharge the capacitive part of the CMUT. This peak current is at least two orders of magnitude higher than the rms current dissipated in the resistive part of the load, hence the capacitive component of the CMUT dominates the power consumption of the output stage. The high-voltage MOS devices in the output stage are sized in order to handle the aforementioned peak current. Designing for this criterion guarantees that the output stage can also supply the current for the resistive part of the CMUT. The widths and lengths of the transistors are shown in Table 1.

Table 1 Output stage transistors W/L

Transistor	W[µm]	L[µm]
M1	700	1.2
M2	700	1.2
M3	400	0.5
M4	400	0.5
M5	700	1.2
M6	400	0.5
M7	10	0.5
M8	10	1.4

Table 2 Level shifters voltages V_{HI} and V_{LO}

Level shifter	Transistor	VLO [V]	VHI [V]
1	M1	87.5	100.0
2	M2	87.5	100.0
3	M3	50.0	62.5
4	M4	50.0	62.5
5	M5	62.5	75.0
6	M6	75.0	87.5

3.2 Level shifters

The control signals of the output stage MOS transistors need to be high-voltage, therefore level shifters are required. The full transmitting circuit requires one level shifter for each output stage MOS transistor, hence a total of six level shifters are used in the design. Each of them operates at different voltages, V_{LO} and V_{HI}, according to the MOS transistor that they are driving. In order to minimize the number of voltage supplies needed for the transmitting circuit the gate-source voltage range of each MOS transistor is set to 12.5 V. The output voltages of each of the six level shifters are shown in Table 2. Note that for the low-voltage input signals lower case notation is used.

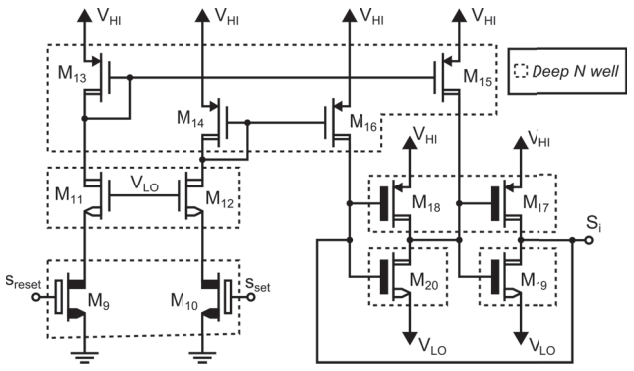

Fig. 6 Schematic of the level shifter. Shared deep N wells indicated with dotted lines.

3.2.1 Design and operation

The level shifter topology used is the pulse-triggered topology that can be seen in Fig. 6. Several variations of this topology have been published [8], [9], [10]. Note that lower case notation is used for the low-voltage input signals (s_{set}, s_{reset}) and upper case notation is used for the high-voltage output signal (S_i). The level shifter consists of a latch formed by M_{17}-M_{20} and two branches to control the latch formed by M_9, M_{11}, M_{13}, M_{15} and M_{10}, M_{12}, M_{14}, M_{16}. The widths and lengths of all the transistors can be seen in Table 3 and the isolation shared deep N wells are clearly indicated in 6. By applying a low-voltage pulse, s_{reset}, with a pulse-width smaller than $1/(2f_r)$ to the gate of M_9 the source of M_{11} is pulled towards ground which also pulls the drain of M_{13} to a lower voltage potential. The current mirror formed by M_{13} and M_{15} transfers a current pulse to the latch, which is a significantly larger current than what M_{20} in the latch can sink which results in S_i being pulled to V_{LO}. Similarly by applying a low-voltage pulse, s_{set}, with a pulse-width smaller than $1/(2f_r)$ to the gate of M_{10} the source of M_{12} is pulled towards ground which also pulls the drain of M_{14} to a lower voltage potential. The current mirror formed by M_{14} and M_{16} transfers a current pulse to the latch, which is a significantly larger current than what M_{19} can sink which results in S_i being pulled to V_{HI}. The main advantage of this pulse-triggered topology is the fact that it only consumes current during the transitions, i.e. when the latch needs to change state. Once the latch level is established, the consumption of the level shifter is zero since the latch automatically maintains the state of S_i. The challenge using this topology is that the latch needs to be very carefully designed in order to correctly define its starting state. This state should match the voltage that turns off the output stage MOS transistor connected to that level shifter. If the starting state is the incorrect one, several output stage MOS transistors might be turned on during the start up which would short circuit two voltage sources.

3.2.2 Device size considerations

The first consideration of this topology is the size of M_9/M_{10} since their width to length ratio should be enough to make sure that the current pulse mirrored in the latch is sufficient to change the state of the latch fast. A width of 10 µm (the minimum allowed in the process) and a length of 2.5 µm (chosen on behalf of the device lifetime) prove to be sufficient to change the latch state. The second consideration is the size of the cascodes M_{11} and M_{12}, which should be large enough to

discharge the PMOS current mirror nodes fast(gates of M_{13}/M_{15} and M_{14}/M_{16} respectively). The minimum device size of 10 µm/3 µm (taking device lifetime into account) was found to be sufficient. The third consideration to be made is the size of M_{13}/M_{14}, which should have a higher saturation drain current than M_9/M_{10} to properly protect the gate-oxide of M_{13}-M_{16} from breakdown. Finally, the latch is sized according to two criteria. The latch is sized asymmetrical in order to have a well-defined initial condition on the start-up which sets the latch to low-voltage (V_{LO}) for the level shifters driving an NMOS in the output stage, or high-voltage (V_{HI}) for the level shifters driving a PMOS in the output stage. Using this approach all the MOS transistors in the output stage will be off in the start-up. Furthermore the switching threshold of the two inverters are set significantly closer to V_{HI} than to V_{LO} which results in a small W/L ratio of the NMOS transistors such that the latch requires as little current from M_{15}/M_{16} to change state as possible. All the MOS devices are sized in order to handle the currents for the worst case corner process, ensuring the functioning of the level shifter independent on the fabrication process.

3.3 Low-voltage logic

The inputs of the Tx circuit carry the information of the pulsing frequency, the driving strength and the waiting, receiving and transmitting time. The functionality of the low-voltage logic is to translate these inputs into the low-voltage signals for the level shifters to correctly drive the output stage. The structure of the low-voltage logic is shown in Fig. 7. Note that lower case notation is used for all the signals of the logic block since they are low-voltage. Firstly, the logic block generates s_1-s_6 which are the low-voltage equivalent of the control signals of the output stage S_1-S_6. Secondly, s_1-s_6 are synchronized using flip-flops, which run at double frequency of pulses ($2f_r$), which also needs to be supplied as an input of the circuit. These flip-flops make sure that even if some small delay is previously added to the input signals due to external routing, the signals s_1'-s_6' sent to the next block are still synchronized. Finally s_1'-s_6' are fed into a pulser circuit that generates the two corresponding s_{set} and s_{reset} impulse signals for the pulse-triggered level shifters previously described. The implementation of the pulser circuit can be seen in Fig. 8. Note that standard cell components are used for all the blocks.

Table 3 Level shifter transistors W/L

Transistor	W[µm]	L[µm]
M9/M10	10	2.5
M11/M12	10	2.0
M13/M14	10	3.0
M15/M16	60	3.0
M17	10	1.1
M18	12	1.1
M19	12	9.0
M20	10	9.0

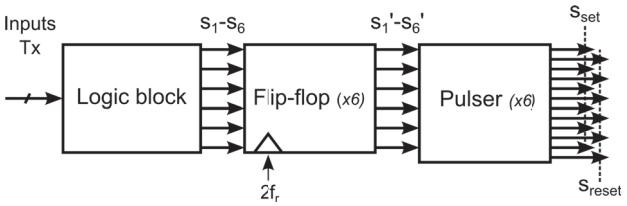

Fig. 7 Low-voltage logic block structure.

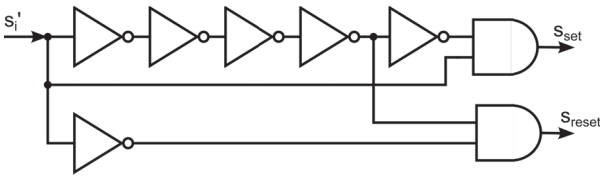

Fig. 8 Pulser circuit schematic used in the low-voltage logic.

4 Measurement results

The transmitting circuit was taped-out in a 0.35 µm high-voltage process and a picture of the integrated circuit taken with a microscope is shown in Fig. 9. Area *a*) contains the transmitting circuit described in this paper which occupies a total space of 0.938 mm^2 and area *b*) contains two copies of the level shifters used in the design for testing and research purposes. Inside the transmitting circuit, the output stage is contained in *c*) with an area of 0.195 mm^2, 20.8%, the level shifters are situated in area *d*) with an area of 0.331 mm^2, 35.3%, and the logic block in area *e*) with an area of 0.011 mm^2, 1.2%. The area in between blocks is routing area, 42.7%, required to connect them together and to connect the inputs and outputs to their corresponding I/O pad.

After the tapeout, a PCB was designed in order to test the functionality of the integrated circuit. Only a single SM 400-AR-8 Delta Elektronika DC power supply, set at 100 V, was connected to the PCB board and the rest of the voltage levels were generated on-board using linear regulators. Linear regulators can not sink current, hence a 470 nF capacitor connected to the output of each linear regulator is added in order to handle any current coming from the integrated circuit. A very small neglectable voltage change of approximately 2 mV is estimated due to the current sinking in the capacitor. The current consumption of the linear regulators

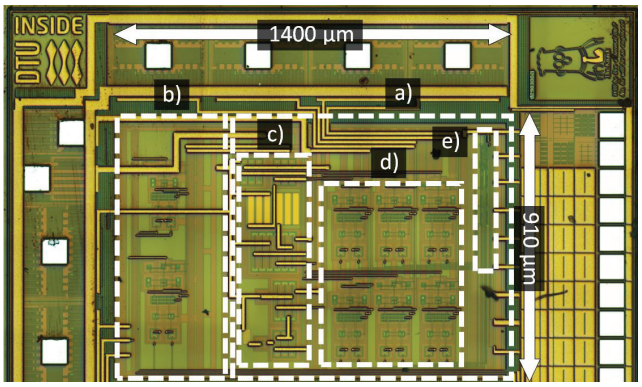

Fig. 9 Picture of the taped-out transmitting circuit. a) Tx circuit. b) Level shifters test. c) Output stage. d) Level shifters. e) Logic block.

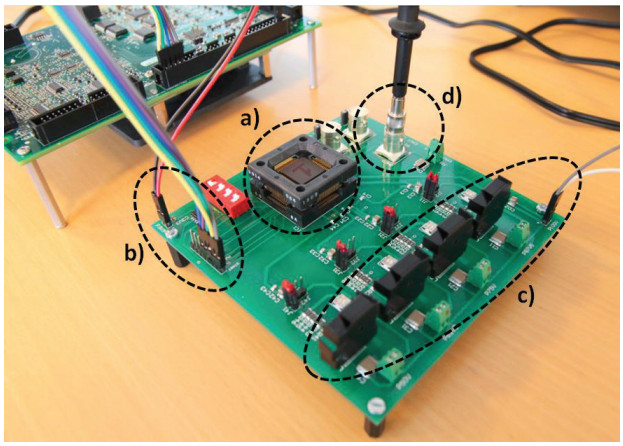

Fig. 10 Setup for the integrated circuit measurements. a) Integrated circuit. b) Xilinx Spartan-6 LX45 FPGA low-voltage signals and low-voltage supply. c) High-voltage supply from a SM 400-AR-8 Delta Elektronika and linear regulators. d) Probe connected to the WaveSurfer 104MXs-B Lecroy oscilloscope.

was not taken into an account, and the power calculations were performed as if the currents supplying the integrated circuit were coming from separate voltage sources instead of a single 100 V source. The low-voltage input signals were supplied using an external Xilinx Spartan-6 LX45 FPGA and the output of the transmitting circuit V_{CMUT} was measured with a WaveSurfer 104MXs-B Lecroy oscilloscope. The transmitting circuit was tested with the most strict frequency and voltage requirements defined in Section 2 and the transmitting, waiting and receiving times were set to 2 µs, 0.2 µs and 1.8 µs respectively. This is equivalent to a 50% transmitting duty cycle which is when the circuit consumes current. A capacitive load of 15 pF corresponding to the capacitive component of the CMUT was connected to the output. The resistive component of the CMUT was not added since it is the current delivered to the capacitive component that determines the output stage power consumption. The measurement setup can be seen in Fig. 10.

The output voltage of the Tx measured on an oscilloscope is shown in Fig. 11 where the fast MOS transistors M_1/M_3 are used in Fig.11 a) and the slow MOS transistors M_2/M_4 are used in Fig. 11 b). The high-voltage transmitting circuit functions as expected, and can achieve the driving speed flexibility desired. However, in low slew rate, the driving strength is not enough to reach the top and bottom voltage rails. R_2 and R_4 were intendedly oversized in order to visually see the different driving speeds in an oscilloscope, however, in simulations, the output was reaching the voltage rails. This mismatch between simulations and measurements is attributed to the parasitics which decrease even further the slew rate. In case that this was a critical issue for a certain transducer, R_2 and R_4 should be reduced, compensating for the parasitics and allowing the output of the Tx to reach full voltage range.

In order to have an idea of the power consumption of the circuit, the currents drawn from each voltage source are measured while driving a capacitive load simulating the CMUT of approximately 15 pF. The power consumption of the transmitting circuit operating at maximum requirements with a 50% transmitting duty cycle is 188 mW. However, this transmitting circuit needs to be used in ultrasound scanners which transmit for a short period of time and then receive for a much longer time which is set by the maximum focus depth of the scanner. Furthermore, ultrasound scanners contain hundreds of CMUTs and each of them require a transmitting circuit. Assuming an ultrasound scanner with 128 CMUTs and maximum focus depth of 10 cm, which leads to a transmitting duty cycle of approximately 1/266, the estimated power consumption of a 128-element transmitting circuit array would be 181 mW.

A comparison table of the design with the state of the art high-voltage integrated transmitting circuits has not been included since, in all of the publications found, the key information such as area and power consumption of the transmitting circuit is unclear, lacking or only specified for receiving circuitry [5],[6],[7],[11].

The circuit is easily reconfigurable by setting externally different frequencies, number of pulses, waiting and receiving times and voltages. During operation, the Tx can be switched on and off without the need of restarting the whole setup, or even switch between M_1/M_2 and M_3/M_4 independently. The target of this paper of designing and implementing an integrated reconfigurable high-voltage transmitting circuit was successfully achieved.

5 Discussion and future improvements

The design presented in this paper can not be directly compared with state of the art Tx circuits since the references found do not specify the driving conditions and individual area and power consumption of the transmitting circuit [5], [11], [12]. Even though the target of the transmitting circuit has been achieved, if this design should be used in an ultrasound scanner the power consumption and area should be reduced. Ultrasound scanners contain thousands of transmitting circuits therefore their power consumption and area need to be scalable.

The first step would be to fix the characteristics of the CMUT that the Tx is designed to drive therefore all the reconfigurability features, which were already acknowledged of having a significant cost in area and power consumption, should be removed. The voltage levels, frequency, driving strength and the operating cycle would be fixed by the transducer characteristics hence the transmitting circuit would be optimally designed regarding its area and power consumption. Improvements can be achieved even if it is assumed that the CMUT to drive has the maximum specifications that the current Tx circuit can drive. In the output stage designed the driving strength was adjustable by using either M_1/M_3 or M_2/M_4 to pulse, hence if the driving strength is fixed, two of the output stage mosfets would be removed decreasing the area of the output stage by approximately 15%. The number of level shifters required would also be reduced by two, achieving an area shrinking in that block of approximately 30%. The logic block would also be simplified, however, since its area is significantly smaller than the other blocks, the area reduction is negligible. The total area reduction estimated of the Tx circuit would be 15%.

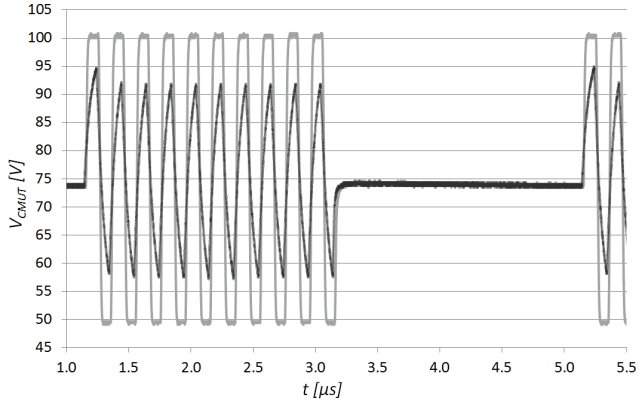

Fig. 11 Output voltage V_{CMUT} measured on the integrated circuit. Plotted data taken from WaveSurfer 104MXs-B Lecroy oscilloscope. a) Fast transitions in light grey. b) Slow transitions in dark grey.

In addition to the previous system design improvements, there are also topology improvements to be done in the most area and power consuming blocks of the system which are the output stage and the level shifters.

Firstly, assuming that non-zero voltage towards the patient is not an issue, it would be interesting to investigate a transmitting circuit that high-voltage biases one of the plates of the transducer and pulse the other. CMUTs are non-polarized devices therefore by applying 100 V to one of the terminals, the pulse required in the other terminal to achieve the same differential voltage between plates of the CMUT only ranges from 0-50 V. Reducing the pulsing voltage levels would lower the maximum absolute voltage that a terminal of an output stage transistor would need to handle hence 50 V transistors could be used instead of 120 V ones. These transistors are around 50% smaller and add less capacitances to charge and discharge therefore both the area and the power consumption of the output stage would improve.

In this design, a three voltage level output stage was used. Two of the levels were used for pulsing and the third level was used as a biasing feature. However, having access to a third voltage level can provide other advantages such as three-level pulsing, which can improve the efficiency of the transmitting circuit [13]. Using this approach would require to remove R_6 in order not to break the driving symmetry required by the CMUT. Another branch connected to $V_{CMUT,MID}$ would be necessary to receive. Additionally, the low-voltage control signals and the low-voltage logic block would need to be changed.

The last improvement suggested for the output stage is the differential driving. Being able to apply voltage to both terminals of the transducer would also make other output stage topologies viable. Particularly, differential driving topologies seem to have advantages compared to the current single ended driving topology. If the CMUT is pulsed from both terminals (differential driving), the pulse swing that each terminal needs to handle is halved, lowering the maximum V_{DS} that the output stage transistors need to handle in each side. Devices with less voltage requirements, which inherently are smaller and have less parasitic capacitances, could be used in these differential topologies hence they will be investigated in the future.

The first approach that could be used in order to improve the level shifters is to reduce the gate-source voltage swing of the output stage MOS transistors from 12.5 V to 5 V. It would increase the number of DC voltage supplies needed for the circuit but it would allow the floating current mirror and the latch of the level shifter to be collected in one single deep N-well resulting in

a considerable area reduction. In addition to fewer N-wells, the 5 V gate-oxide transistors can have a considerably smaller width compared to the thick gate-oxide transistors used in the current level shifter design. The estimated area reduction per level shifter is 50%. Using this reduced voltage swing, the output stage transistors would also receive a reduced gate voltage swing therefore 5 V gate-oxide devices could also be used instead of the thick gate-oxide ones saving even more area.

Using all the topology improvements suggested for both the output stage and the level shifters, it is estimated that a redesigned transmitting circuit with the same specifications would occupy an on-chip area of 0.45 mm^2. The expected power consumption of a redesigned 128-element transmitting circuit array would be approximately 105 mW.

6 Conclusions

In this paper a reconfigurable high-voltage transmitting circuit for CMUTs was designed and implemented in a 0.35 µm high-voltage process. The pulsing frequency, driving speed, voltage levels and the transmitting, waiting and receiving time are easily adjustable externally making it suitable for CMUTs with very different specifications. The on-chip area occupied by the Tx circuit designed is 0.938 mm^2. The highest driving capabilities of the Tx circuit are a maximum voltage of 100 V, a maximum peak-to-peak pulse voltage swing of 50 V and a frequency of 5 MHz. Operating at these maximum specifications, the power consumption of a 128-element transmitting circuit array is 181 mW for a 15 pF CMUT load. In the future, several ideas and improvements to reduce the power consumption and area of the transmitting circuit are going to be tested and implemented. The expected on-chip area of a new design with the suggested improvements is 0.45 mm^2 and the estimated power consumption of a new 128-elements transmitting circuit array is 105 mW.

References

1. Arif. S.Ergun, Goksen G. Yaralioglu and Butrus T. Khuri-Yakub, "Capacitive Micromachined Ultrasonic Transducers: Theory and Technology" in *Journal of Aerospace Engineering*, pp.74-87 (2013)
2. G. Gurun, P. Hasler and F.L. Degertekin, "Front-End Receiver Electronics for High- Frequency Monolithic CMUT-on-CMOS Imaging Arrays" in *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, Vol. 58, No. 8, pp.1658-1668 (2011)
3. Butrus T. Khuri-Yakub and Ömer Oralkan, "Capacitive micromachined ultrasonic transducers for medical imaging and therapy" in *Journal of Micromechanics and Microengineering*, Vol. 21, pp.1-11 (2011)
4. P. Llimós Muntal, D. Ø. Larsen, I. H.H. Jørgensen and E. Bruun, "Integrated Reconfigurable High-Voltage Transmitting Circuit for CMUTs" in *32nd Norchip Conference* (2014)
5. G. Gurun, P. Hasler and F.L. Degertekin, "A 1.5-mm Diameter Single-Chip CMOS Front-End System with Transmit-Receive Capability for CMUT on-CMOS Forward-Looking IVUS" in *IEEE International Ultrasonics Symposium Proceedings*, pp.478-481 (2011)
6. I.O. Wygant, X. Zhuang, D.T. Yeh, A. Nikoozadeh, . Oralkan, A.S. Ergun, M. Karaman and B.T. Khuri-Yakub, "An Endoscopic Imaging System Based on a Two-Dimensional CMUT Array: Real-Time Imaging Results" in *IEEE Ultrasonic Symposium*, pp.792-795 (2005)
7. D. Zhao, M. Tong Tan, H.-Kyu Cha, J. Qu, Y. Mei, HaoYu, A. Basu, M. Je, "High-voltage Pulser for Ultrasound Medical Imaging Applications" in *International Symposium on Integrated Circuits*, pp.408-411 (2011)
8. H. Ma, R. van der Zee, and B. Nauta, "Design and Analysis of a High-Efficiency High-Voltage Class-D Power Output Stage" in *Solid-State Circuits, IEEE Journal*, vol.49, no.7, pp.1514-1524 (2014)
9. T. Lehmann, "Design of fast low-power floating high-voltage levelshifters" in *Electronics Letters*, vol.50, no.3, pp.1 (2014)
10. D. Liu, S. J. Hollis, and B. H. Stark, "A new circuit topology for floating high voltage level shifters" in *Microelectronics and Electronics (PRIME), 10th Conference on Ph.D. Research*, pp.1-4 (2014)
11. I.O. Wygant, X. Zhuang, D.T. Yeh, . Oralkan, A.S. Ergun, M. Karaman and B.T. Khuri-Yakub, "Integration of 2D CMUT Arrays with Front-End Electronics for Volumetric Ultrasound Imaging" in *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, Vol. 55, No. 2, pp.327-342 (2008)
12. Sung-J. Jung, Jong-K. Song and Oh-K. Kwon, "Three-Side Buttable Integrated Ultrasound Chip With a 16 16 Reconfigurable Transceiver and Capacitive Micromachined Ultrasonic Transducer Array for 3-D Ultrasound Imaging Systems" in *IEEE Transactions on Electron Devices*, Vol. 60, No. 10, pp.3562-3569 (2013)
13. K. Chen, H-S. Lee, A.P. Chandrakasan and C.G. Sodini, "Ultrasonic Imaging Transceiver Design for CMUT: A Three-Level 30-Vpp Pulse-Shaping Pulser With Improved Efficiency and a Noise-Optimized Receiver" in *IEEE Journal of Solid-State Circuits*, Vol. 48, No. 11, pp.2734-2745 (2013)